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EXAMINER	
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ART UNIT	**PAPER NUMBER**
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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/034,734	LI ET AL.	
	Examiner	Art Unit	
	Charles C. Chow	2685	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *9/13/2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-46* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14,17 and 19-26* is/are rejected.

7)☒ Claim(s) *15,16 and 18* is/are objected to.

8)☒ Claim(s) *27-46* are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 December 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *5, 6*.
4) ☒ Interview Summary (PTO-413) Paper No(s)/Mail Date. *7*.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Detailed Action

Election/Restriction

1. Restriction to one of the following inventions is required under 35 U.S.C. § 112: I. Claims

   I. Claims 1-26 are drawn to automatic gain control, gain control loop and DC offset loop, classified in class 455, subclass 232.1 to 251.1.

   II. Claims 27-32 are drawn to control message routing using serial bus, classified in class 455, subclass 412.2.

   III. Claims 34-38 are drawn to receiver, digital processor, and serial bus, classified in class 455, subclass 550.1.

   IV. Claims 39-46 are drawn to wireless system, receiver with digital variable amplifier DVGA, AGC, DC offset, classified in class 455, subclass 403,127.2, 63.1.

2. The inventions are distinct, each from the other because of the following reasons:

   Inventions [I], [II], [III], [IV] are related as combination and subcombination. Inventions in this relationship are distinct if it can be shown that (1) the combination as claimed does not require the particulars of the subcombination as claimed for patentability, and (2) that the subcombination has utility by itself or in other combinations (MPEP § 806.05 (C)). In the instant case, the combination as claimed does not require the particulars subcombination in the other group for the claims. The subcombination in the each group I, II, III, IV, are having distinct subcombination which is different from the other group, as shown above.

3. Because these inventions are distinct for the reasons given above and have acquired a separate status in the art because of their recognized divergent subject matter, restriction for examination purposes as indicated is proper.

4. Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 C.F.R. § 1.48 (b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a deligently-filed petition under 37 C.F.R. § 1.48 (b) and by the fee required under 37 C.F.R. § 1.17 (h).

5. During a telephone conversation with attorney George Pappas, 9/13/04 to 9/14/04, a emailed document received, for a provisional election was made without traverse to prosecute the invention of group I, claims 1-26. Affirmation of this election must be made by applicant in replying to this Office action. Claims 27-46, withdrawn from further consideration by the examiner, 37 C.F.R. 1.142(b), as being drawn to a nonelected invention.

Specification-Title

6. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed. The current title does not describe automatic gain controlling, AGC loop, and DC offset loop for DC offset correction.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -
(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Fagan (GB 2,229,333A).

Regarding **claim 1**, Fagan teaches an automatic gain control AGC apparatus (Fig. 1-2, abstract), an analog variable gain amplifier AVGA (coarse gain control element 14 for receiving analog signal with variable gain control G1, B, Fig. 1, page 6, lines 1-16), a digital variable gain amplifier DVGA (element 17 for amplifying 12-bit digital signal from ADC 16, Fig. 1, page 6, lines 23-30), coupled to an output of the analog variable gain amplifier AVGA (the element 17 coupled to element 14 via 16 ADC, Fig. 1), and a gain controller (proecessor 15) adapted to measure a signal output from the DVGA (the processor 15 receives V' from 18' for estimate the DVGA 17 output at 12, page 7, lines 15-27), and to control the gains of the analog and digital variable gain amplifiers (the processor 15 provides control b to ADVA 14 and control signal G2 to DVGA 17, page 7, line 28 to page 8, line 34).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:
A person shall be entitled to a patent unless -

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

8. Claims 3, 6, 11-12 are rejected under 35 U.S.C. 102(e) as being anticipated by Ruelke (US 6,459,889 B1).

Regarding **claim 3**, Ruelke teach a method of operating an automatic gain control AGC loop in combination with a DC loop (the AGC loop formed by 140, 122, 158; the DC loop

formed by 160, 162, 164 and 186,168,170, Fig. 1, abstract), selecting a particular DC operating mode for the DC loop from among a plurality of possible DC operating modes, operating the DC loop in the selected DC operating mode to correct for DC offset in a desired signal (the DC operating modes in steps 344, 348, 352, Fig. 3B, for non-slotted system mode, to initiate digital correction sequence to correct DC baseband offset, and the DC operating mode in steps 384, 376, 378, 382, for the slotted system mode, to initiate a binary search to correct baseband DC in step 378; the first DE offset correction sequence for non-slotted protocol and the second DC offset correction sequence for slotted protocol in col. 12, lines 31-55; the DC offset correction for slotted protocol and different strategies for non-slotted protocol, in col. 5, lines 26-40), selecting a particular AGC operating mode for the AGC loop from among a plurality of possible AGC operating modes based on the selected DC operating mode and operating the AGC loop in the selected AGC operating mode to provide variable gain for the desired signal (for the non-slotted protocol, the first DC offset correction sequence comprises the presetting a DC offset correction and allowing an, particular, AGC loop to respond while DC offset correction loop is correcting the DC offset, and for the slotted protocol, the second DC offset correction sequence, setting the AGC to a value which eliminates on-channel input signals and carrying out a Dc offset correction to restore normal AGC operation in col. 12, lines 17-55; the AGC in steps 376-382 for slotted protocol, the AGC in steps 344-352 for non-slotted protocol in Fig. 3B).

Regarding **claim 6**, Ruelke teaches the plurality of possible AGC operating modes (signal (the plurality of AGC operating modes for slotted and non-slotted environment and protocols, abstract, col. 3, lines 31-53; col. 5, lines 26-54, Fig. 3B), is associated with a

respective AGC loop gain (the associated AGC loop gain setting in slotted protocol for 10 db in step 376, and then reset AGC for nominal operation using fast AGC in step 382, Fig. 3B; the associated AGC loop gain setting in the non-slotted protocol for initial condition IC in step 344, and then simultaneous AGC setting while correcting DC offset in step 352).

Regarding **claim 11**, Ruelke teaches a receiver in a wireless communication system (the receiver in abstract, Fig. 1, the Zif, DCR receiver in col. 3, lines 31-41, for AMPS, TDMA system, col. 5,lines 42-55; col. 7, lines 62-67), comprising a DC loop configurable to operate in one of a plurality of possible DC operating modes to correct for DC offset in a desired signal (the both AGC and DC offset correction loop DOCL are dynamically configured for optimum complimentary operation via microprocessor 236 and serial bus, Fig. 2, depending on the receiver's operating environment and protocol, abstract; the plurality of DCOCL operating modes for slotted protocol and non-slotted protocol, col. 3, lines 31-53; col. 5, lines 26-54, Fig. 3B), and An AGC loop configurable to operate in one of a plurality of possible AGC operating modes to variable gain for the desired signal (the plurality of AGC operating modes for slotted and non-slotted environment and protocols, abstract, col. 3, lines 31-53; col. 5, lines 26-54, Fig. 3B), wherein the particular AGC operating mode to be used is determined based on the particular DC operating mode selected for use for the DC loop (for the non-slotted protocol, the first DC offset correction sequence comprises the presetting a DC offset correction and allowing an, selected particular, AGC loop to respond while DC offset correction loop is correcting the DC offset, and for the slotted protocol, the second DC offset correction sequence, setting the , selected particular, AGC to a value which eliminates on-channel input signals and carrying out a DC offset correction to restore normal

AGC operation in col. 12, lines 17-55; the AGC in steps 376-382 for slotted protocol, the AGC in steps 344-352 for non-slotted protocol in Fig. 3B).

Regarding **claim 12**, Ruelke teaches an control apparatus (microprocessor 236, serial bus 242, Fig. 2) in a wireless communication system (the AMPS, TDMA system in col. 5, lines 42-55; col. 7, lines 62-67), comprising means for selecting a particular DC operating mode for a DC loop from among a plurality of possible DC operating modes (the both AGC and DC offset correction loop DOCL are dynamically configured for optimum complimentary operation via microprocessor 236 and serial bus, Fig. 2, depending on the receiver's operating environment and protocol, abstract; the plurality of DCOCL operating modes for slotted protocol and non-slotted protocol, col. 3, lines 31-53; col. 5, lines 26-54, Fig. 3B), means for operating the DC loop in the selected DC operating mode to correct for DC in the desired signal (the DC operating modes in steps 344, 348, 352, Fig. 3B, for non-slotted system mode, to initiate digital correction sequence to correct DC baseband offset, and the DC operating mode in steps 384, 376, 378, 382, for the slotted system mode, to initiate a binary search to correct baseband DC in step 378; the first DC offset correction sequence for non-slotted protocol and the second DC offset correction sequence for slotted protocol in col. 12, lines 31-55; the DC offset correction for slotted protocol and different strategies for non-slotted protocol, in col. 5, lines 26-40), means for selecting a particular AGC operating mode for an AGC loop from among a plurality of possible AGC operating modes base on the selected DC operating mode and means for operating AGC loop in the selected AGC operating mode to provide variable gain for the desired signal (the plurality of AGC operating modes for slotted and non-slotted environment and protocols, abstract, col. 3, lines 31-53; col. 5, lines 26-54,

Fig. 3B, the non-slotted protocol, the first DC offset correction sequence comprises the presetting a DC offset correction and allowing an, selected particular, AGC loop to respond while DC offset correction loop is correcting the DC offset, and for the slotted protocol, the second DC offset correction sequence, setting the , selected particular, AGC to a value which eliminates on-channel input signals and carrying out a DC offset correction to restore normal AGC operation in col. 12, lines 17-55; the AGC in steps 376-382 for slotted protocol, the AGC in steps 344-352 for non-slotted protocol in Fig. 3B).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Fagan in view of Becker et al. (US 5,612,975) and Webster et al. (US 6,748,200 B1).

Regarding **claim 2**, Fagan fail to teach a DC offset canceller interposed between the output of the analog variable gain amplifier AVGA and an digital variable gain amplifier DVGA. However, Becker et al. (Becker) teaches this features, the DC bias remover 235 between variable amplifier 206, the wide band AGC 280 and post detection AGC digital amplifier 248 (col. 9, lines 17-22, col. 9, line 61 to col. 10, line 20, Fig. 9, Fig. 13, col. 13, lines 36-62). Becker fails to teach the AGC loop gain varies according to the operating mode of the DC offset canceller. Webster teaches teach the AGC loop gain varies according to the

operating mode of the DC offset canceller, the AGC/DC control 141 (Fig. 1) generate GC to adjust the gain for AVGA, BB-AGC 125, via 147, 151, and generating GDADJ for adjusting the DVGA 135 (col. 8, lines 29-36; col. 8, line 59 to col. 9, line 29), according to the DC offset input to 139 BB-DC offset and signal power estimate, the DCE output from 139 to 141 (col. 8, line 37 to col. 10, line 60). Webster teaches the AGC system having the DC control loop for the ZIF of a wireless communication device (col. 1, lines 20-27), for improving of the DC offset error in a short time associated with an AGC procedure (col. 2, lines 43-64). Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to modify Fagan with Becker's fast DC offset removal with AGC, such that the DC offset could be quickly removed in the AGC loop for a wireless communication device.

10. Claims 4-5, 13-14, 17, 19-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ruelke in view of Dutkiewicz et al. (US 5,629,960).

Regarding **claim 4**, Ruelke fails to teach the DC operating modes including an acquisition mode and tracking mode. However, Dutkiewicz et al. (Dutkiewicz) teaches the acquisition mode for DC offset correction by utilizing acquire input at DC tracking 23 (Fig. 3) from control 26 (col. 3, lines 52-61, the acquire mode for rapid tracking, col. 5, lines 28-44), the DC offset tracking mode input to DC tracking 23, the wider bandwidth in acquire mode for quick synchronization, the narrow bandwidth for DC offset tracking mode to reduce noise (col. 3, line 44 to col. 4, line 26), the large DC offset shift (col. 4, lines 50-58). Dutkiewicz teaches reducing the distortion effect on the DC offset due to large transient, to improve the symbol clock synchronization effect (col. 1, line 61 to col. 2, lines 46), by utilizing the wide

bandwidth acquisition mode and narrow bandwidth tracking mode. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to modify Ruelke with Dutkiewicz's acquisition mode and tracking mode, such that the receiver could track the time information by removing the DC offset distortion.

Regarding **claim 5**, Dutkiewicz teaches the acquisition mode has a wider loop bandwidth than that of the tracking mode, and is used to more quickly remove a large DC offset in the desired signal (col. 3, line 44 to col. 4, line 26; the large DC offset shift (col. 4, lines 50-58).

Regarding **claim 13,** Ruelke teaches a method of operating DC loop in a receiver unit (the DC operating loop for correcting DC offset in different protocol modes, for the slotted and non-slotted protocol in Fig. 3B, and in col. 3, col. 5, col. 12; the ZIF, DCR receiver, col. 3, line 34-35), selecting a particular operating mode for the DC loop from among a plurality of possible operating modes (the DC operating modes in steps 344, 348, 352, Fig. 3B, for non-slotted system mode, to initiate digital correction sequence to correct DC baseband offset, and the DC operating mode in steps 384, 376, 378, 382, for the slotted system mode, to initiate a binary search to correct baseband DC in step 378; the first DE offset correction sequence for non-slotted protocol and the second DC offset correction sequence for slotted protocol in col. 12, lines 31-55; the DC offset correction for slotted protocol and different strategies for non-slotted protocol, in col. 5, lines 26-40). Ruelke fails to teach the operating the DC loop in the selected acquisition mode for the particular time duration to correct for DC offset wherein the particular time duration is inversely proportional to a loop bandwidth for the DC loop for the acquisition mode. However, Dutkiewicz teaches the operating the DC

loop in the selected acquisition mode for the particular time duration to correct for DC offset wherein the particular time duration (the particular time during acquire mode using wider DC offset loop bandwidth for quick synchronization, col. 3, lines 56-61), the short time 10-20 milliseconds, for the particular time duration is inversely proportional to a loop bandwidth (col. 5, lines 31-32), the transitioning out of the acquisition mode after the particular time duration (the until a short time after the Tx/off, typically 10-20 milliseconds, col. 5,l ines 28-32). Dutkiewicz teaches reducing the distortion effect on the DC offset due to large transient, to improve the symbol clock synchronization effect (col. 1, line 61 to col. 2, lines 46), by utilizing the wide bandwidth acquisition mode and narrow bandwidth tracking mode, for the DC offset correction loop. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to modify Ruelke with Dutkiewicz's wide bandwidth acquisition mode and narrow bandwidth tracking mode, such that the receiver could track the time information by removing the DC offset distortion.

Regarding **claim 14**, Dutkiewicz teaches the acquisition mode is selected in response to an event to result in a large DC offset in the desired signal (col. 3, line 53 to col. 4, line 26; col. 4, lines 50-58).

Regarding **claim 17**, Dutkiewicz teaches the possible tracking mode (42, 23, Fig. 3, col. 2, lines 30-37; col. col. 3, lines 49-57).

Regarding **claim 19**, Dutkiewicz teaches the particular time duration is selected based on an expected amplitude of the DC offset in the desired signal (the particular time just before key on time and until a short time after the key off, col. 2, lines 30-37).

Regarding **claim 20**, Dutkiewicz teaches the particular time duration is further selected to

minimize a combination of DC offset introduced in the desired signal (the time duration for wide bandwidth acquire mode for quick synchronization in col. 3, lines 57-61) and loop noise from DC loop (the reducing nose on the tracking sub-system, col. 3, lines 53-57, for the time duration for narrow band tracking mode)

Regarding **claim 21**, Ruelke teaches the DC loop in a receiver (receiver in abstract, col. 3, lines 34-35, the DC loop 160,162,164, 186,168, 170, Fig. 1). Ruelke fails to teach a summer. However, Dutkiewicz teaches a summer operative to subtract a DC offset value form the desired signal to provide a DC offset corrected signal (22, Fig. 3, col. 3, line 32-37), a loop control unit (26) configurable to operate in one of a plurality of possible operating modes to provide the DC offset value (the plurality of operating modes, track, or acquire, to DC tracking 23, Fig. 3), wherein the plurality of possible operating modes include the acquisition mode having particular wide bandwidth (Fig. 3, col. col. 3, lines 44-61), wherein the loop control unit is operated in the acquisition mode (the controller 26 has DC offset mode select 42, Fig. 3), wherein the particular time duration (the particular time during acquire mode using wider DC offset loop bandwidth for quick synchronization, col. 3, lines 56-61), the short time 10-20 milliseconds, for the particular time duration is inversely proportional to a loop bandwidth (col. 5, lines 31-32), the transitioning out of the acquisition mode after the particular time duration (the until a short time after the Tx/off, typically 10-20 milliseconds, col. 5, lines 28-32). Dutkiewicz teaches reducing the distortion effect on the DC offset due to large transient, to improve the symbol clock synchronization effect (col. 1, line 61 to col. 2, lines 46), by utilizing the wide bandwidth acquisition mode and narrow bandwidth tracking mode, for the DC offset correction loop. Therefore, it would have been obvious to one of

ordinary skill in the art at the time of invention to modify Ruelke with Dutkiewicz's wide bandwidth acquisition mode and narrow bandwidth tracking mode, such that the receiver could track the time information by removing the DC offset distortion.

Regarding **claim 22**, Ruelke teaches an apparatus in receiver (the DCOCL in receiver in abstract, col. 3, lines 34-35, the DC loop 160,162,164, 186,168, 170, Fig. 1). Ruelke teaches means for selecting a particular operating mode for DC loop (steps in Fig. 3B, for the DC operating modes for slotted protocol or non-slotted protocol). Ruelke fails to teach the acquisition mode and the means for operating DC loop in the acquisition mode for a particular time duration, (Fig. 3, col. col. 3, lines 44-61), wherein the loop control unit is operated in the acquisition mode (the controller 26 has DC offset mode select 42, Fig. 3), wherein the particular time duration (the particular time during acquire mode using wider DC offset loop bandwidth for quick synchronization, col. 3, lines 56-61), the short time 10-20 milliseconds, for the particular time duration is inversely proportional to a loop bandwidth (col. 5, lines 31-32), the transitioning out of the acquisition mode after the particular time duration (the until a short time after the Tx/off, typically 10-20 milliseconds, col. 5, lines 28-32). Dutkiewicz teaches reducing the distortion effect on the DC offset due to large transient, to improve the symbol clock synchronization effect (col. 1, line 61 to col. 2, lines 46), by utilizing the wide bandwidth acquisition mode and narrow bandwidth tracking mode, for the DC offset correction loop. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to modify Ruelke with Dutkiewicz's wide bandwidth acquisition mode and narrow bandwidth tracking mode, such that the receiver could track the time information by removing the DC offset distortion.

11. Claim 7 is are rejected under 35 U.S.C. 103(a) as being unpatentable over Ruelke in view of Sutterlin et al. (US 5,463,662).

Regarding **claim 7,** Ruelke teaches the reset AGC for nominal operation using fast AGC (step 382, Fig. 3B). Ruelke fails to teach the low gain mode in the AGC operating modes. However, Sutterlin et al. (Sutterlin) teaches the low gain mode in the AGC operating modes (the AGC state diagram having the high gain state, Fig. 6, col. 12, lines 10-14; the low gain state, Fig. 6, col. 12, lines 43-56; col. 11, lines 15-45), for reducing gain error due to noise (col. 1, line 20 to col. 2, line 9). Ruelke suggest AGC control but not the low gain mode. Sutterlin teaches the low gain mode for reducing the noise effect on the received signal. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to modify Ruelke with Sutterlin's low gain state, such that the receiver could reduce the noise signal.

12. Claim 8 is are rejected under 35 U.S.C. 103(a) as being unpatentable over Ruelke in view of Sutterlin, as applied to claim 7 above, and further in view of Heck et al. (US 5,483,691).

Regarding **claim 8,** Ruelke and Sutterlin fail to teach the freeze mode in AGC operating modes, although Sutterlin teaches the improved technique for better signal to noise ratio in the AGC system (col. 1, lines 26-50). However, Heck et al. (Heck) teaches the freeze mode for AGC operating mode, the limiting the gain reduction upon gain control signal reaching a predetermined gain reduction limit threshold, for providing improved signal to noise ratio (col. 1, line 59 to col. 2, line 4, abstract), for the freezing mode of the AGC operation at the

gain limit threshold. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to modify Ruelke with Heck's the limiting gain reducing at predetermined threshold, such that the receiver could provide the improved signal to noise ratio.

13. Claim 9 is are rejected under 35 U.S.C. 103(a) as being unpatentable over Ruelke in view of Dutkiewicz, as applied to 4 above, and further in view of Sutterlin-'662.

Regarding **claim 9,** Dutkiewicz teaches the acquire mode for the DC operating mode (42, DC tracking 23, Fig. 3). Ruelke teaches the AGC modes for slotted and non-slotted protocols. Ruelke and Dutkiewicz fail to teach the selected AGC operating mode is a low gain mode when selected DC operating mode is the acquisition mode. However, Sutterlin teaches the low gain mode for the AGC states in Fig. 6. for preventing the noise interference (col. 1, line 20 to col. 2, line 9). Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to modify Ruelke and Dutkiewicz with Sutterlin's low gain state, such that such that the receiver could reduce the noise signal.

14. Claim 10 is are rejected under 35 U.S.C. 103(a) as being unpatentable over Ruelke in view of Dutkiewicz, as applied to claim 4 above, and further in view of Heck-'691.

Regarding **claim 10** Dutkiewicz teaches the acquire mode for the DC operating mode (42, DC tracking 23, Fig. 3). Ruelke teaches the AGC modes for slotted and non-slotted protocols. Ruelke and Dutkiewicz fail to teach the selected AGC operating mode is a freeze mode when selected DC operating mode is the acquisition mode. However, Heck teaches the

freeze mode for AGC operating mode, the limiting the gain reduction upon gain control signal reaching a predetermined gain reduction limit threshold, for providing improved signal to noise ratio (col. 1, line 59 to col. 2, line 4, abstract), for the freezing mode of the AGC operation at the gain limit threshold. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to modify Ruelke and Dutkiewicz with Heck's the limiting gain reducing at predetermined threshold, such that the receiver could provide the improved signal to noise ratio.

15. Claims 23-24, 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fagan in view of Kotzian (US 5,014,013).

Regarding **claim 23,** Fagan teaches a method of digitally amplifying a desired signal (the fine gain control element 17 for digitally amplifying signal received from ADC 16, page 6, lines 23-30), receiving a gain represented in a logarithm format (the received G1, G2, in dBV of the logarithm format, page 12, lines 4-21), determining a different between the received gain and a gain offset (the received gain V' and desired output level 11 are compared for difference in element 20 and sending gain error value to processor 15, Fig. 1, page 7, line 15 to page 8, line 35), digitally multiplying the desired signal with the output gain (the digital multiplier in element 17, fine gain control, based on binary value of G2 from processor; the multiplying N factor of the G1 in coarse gain control element 14, page 6, lines 1-30). Fagan fails to teach the converting the difference in logarithm format to an input gain in linear format. However, Kotzian teaches this feature, the antilog 86 for converting received gain error signal to linear gain value for linear amplifier 87, and adding gain in logarithm value is

to multiply gain in linear value (Fig. 2, col. 2, lines 37-66; col. 4, line 32 to col. 5, line 2). Fagan has taught the digital gain control G1, G2 in dBV format, Fagan does not clearly describe whether the G1, G2 gain values are applied to multiplier in logarithm or linear format. Kotzian teaches the antilog circuit for converting the logarithm gain error value to linear format so that the linear value can be conveniently, flexibly, applied to the audio, video, where the linear gain values are needed (col. 1, line 60 to col. 2, line 6). Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to modify Fagan with Kotzian's antilog circuits for converting logarithm gain value to linear gain value, such that the amplifier gain could be corrected by utilizing the required linear gain value.

Regarding **claim 24**, Fagan teaches a method of digitally amplifying a desired signal (the fine gain control element 17 for digitally amplifying signal received from ADC 16, page 6, lines 23-30), receiving a gain represented in a logarithm format (the received G1, G2, in dBV of the logarithm format, page 12, lines 4-21), determining a different between the received gain and a gain offset (the received gain V' and desired output level 11 are compared for difference in element 20 and sending gain error value to processor 15, Fig. 1, page 7, line 15 to page 8, line 35), digitally multiplying the desired signal with the output gain (the digital multiplier in element 17, fine gain control, based on binary value of G2 from processor; the multiplying N factor of the G1 in coarse gain control element 14, page 6, lines 1-30). Fagan fails to teach the converting the difference in logarithm format to an input gain in linear format. However, Kotzian teaches this feature, the antilog 86 for converting received gain error signal to linear gain value for linear amplifier 87, and adding gain in logarithm value is to multiply gain in linear value (Fig. 2, col. 2, lines 37-66; col. 4, line 32 to col. 5, line 2).

Fagan has taught the digital gain control G1, G2 in dBV format, Fagan does not clearly describe whether the G1, G2 gain values are applied to multiplier in logarithm or linear format. Kotzian teaches the antilog circuit for converting the logarithm gain error value to linear format so that the linear value can be conveniently, flexibly, applied to the audio, video, where the linear gain values are needed (col. 1, line 60 to col. 2, line 6). Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to modify Fagan with Kotzian's antilog circuits for converting logarithm gain value to linear gain value, such that the amplifier gain could be corrected by utilizing the required linear gain value. Regarding **claim 26**, Fagan teaches a method of digitally amplifying a desired signal (the fine gain control element 17 for digitally amplifying signal received from ADC 16, page 6, lines 23-30), receiving a gain represented in a logarithm format (the received G1, G2, in dBV of the logarithm format, page 12, lines 4-21), determining a different between the received gain and a gain offset (the received gain V' and desired output level 11 are compared for difference in element 20 and sending gain error value to processor 15, Fig. 1, page 7, line 15 to page 8, line 35), digitally multiplying the desired signal with the output gain (the digital multiplier in element 17, fine gain control, based on binary value of G2 from processor; the multiplying N factor of the G1 in coarse gain control element 14, page 6, lines 1-30). Fagan fails to teach the converting the difference in logarithm format to an input gain in linear format. However, Kotzian teaches this feature, the antilog 86 for converting received gain error signal to linear gain value for linear amplifier 87, and adding gain in logarithm value is to multiply gain in linear value (Fig. 2, col. 2, lines 37-66; col. 4, line 32 to col. 5, line 2). Fagan has taught the digital gain control G1, G2 in dBV format, Fagan does not clearly

describe whether the G1, G2 gain values are applied to multiplier in logarithm or linear format. Kotzian teaches the antilog circuit for converting the logarithm gain error value to linear format so that the linear value can be conveniently, flexibly, applied to the audio, video, where the linear gain values are needed (col. 1, line 60 to col. 2, line 6). Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to modify Fagan with Kotzian's antilog circuits for converting logarithm gain value to linear gain value, such that the amplifier gain could be corrected by utilizing the required linear gain value.

16. Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over Fagan in view of Kotzian, as applied to claim 24 above, and further in view of Wilson (US 5,627,857).

Regarding **claim 25,** Fagan and Koztian fail to teach the multiplexer and wherein the digital multiplier is operating to multiply in phase and quadrature phase input samples in a time division multiplexed manner. However, Wilson teaches this features, the mux 305 for multiplexing in phase I and quadrature Q signal (Fig. 3, col. 4, line 61 to col. 5, line 63), having digital multiplier 405 for multiplying digital gain to the sampled I, Q, RSSI value (Fig. 4, col.5, lines 39-63) in time division multiplexed manner at 38.4 ksamples/ second (col. 5, lines 1-26), which is equivalent to applicant's multiplier 316. Koztian teaches the digital AGC with improved gain error by eliminating the nonlinear errors (col. 2, lines 32-64) and Fagan has taught above the digital gain loop and digital multiplier. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to modify Fagan and Kotzian with Wilson's mux 305, multiplier 405, such that the gain for the AGC loop could be adjusted with improved error by eliminating nonlinear error.

Claims Objection

17. Claims 15-16, 18 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The cited references fail to teaches the features based on claim 13 for the event corresponding to a switch to new analog circuits stages to process the desired signal, and the event corresponding to application of a new DC offset value to correct for static DC offset, by operating the DC loop for acquisition with particular time duration.

Conclusion

18. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

    A. US2003/0100,286 A1, May 2003, assignee, Severson et al. teaches the AGC loop associated with 170, the DC offset loop associated with 140, Fig. 1, abstract, having serial bus interface 160, the digital amplifier 180, the LNA 110 for the direct conversion receiver.

19. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Charles Chow whose telephone number is (703)-306-5615.

    If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Edward Urban, can be reached at (703)-305-4385.

    Any response to this action should be mailed to:

    Commissioner of Patents and Trademarks

    Washington, D.C. 20231

or faxed to: (703) 872-9306 (for Technology Center 2600 only)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

Charles Chow C.C.

September 17, 2004.

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